Refine Search

Search Results -

Terms	Documents
node same (configur$6 near5 ROM) same (serial adj1 bus)	26

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L1

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Monday, March 22, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L1	node same (configur$6 near5 ROM) same (serial adj1 bus)	26	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L1	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L2

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Monday, March 22, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	L1	0	L2
DB=USPT; PLUR=YES; OP=OR			
L1	node same (configur$6 near5 ROM) same (serial adj1 bus)	26	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
(358/1.15 |370/463 |709/253 |709/301 |709/302 |709/220 |710/104 |710/105 |710/106 |710/62 |710/63.2 |710/305 |710/8 |714/1).ccls.	5718

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Monday, March 22, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=YES; OP=OR		
L3	710/104,105,106,62,63.2,305,8;709/253,301,302,220;370/463;714/1;358/1.15.ccls.	5718	L3
	DB=USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L2	L1	0	L2
	DB=USPT; PLUR=YES; OP=OR		
L1	node same (configur$6 near5 ROM) same (serial adj1 bus)	26	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L1 and L3	15

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search | Recall Text | Clear | Interrupt

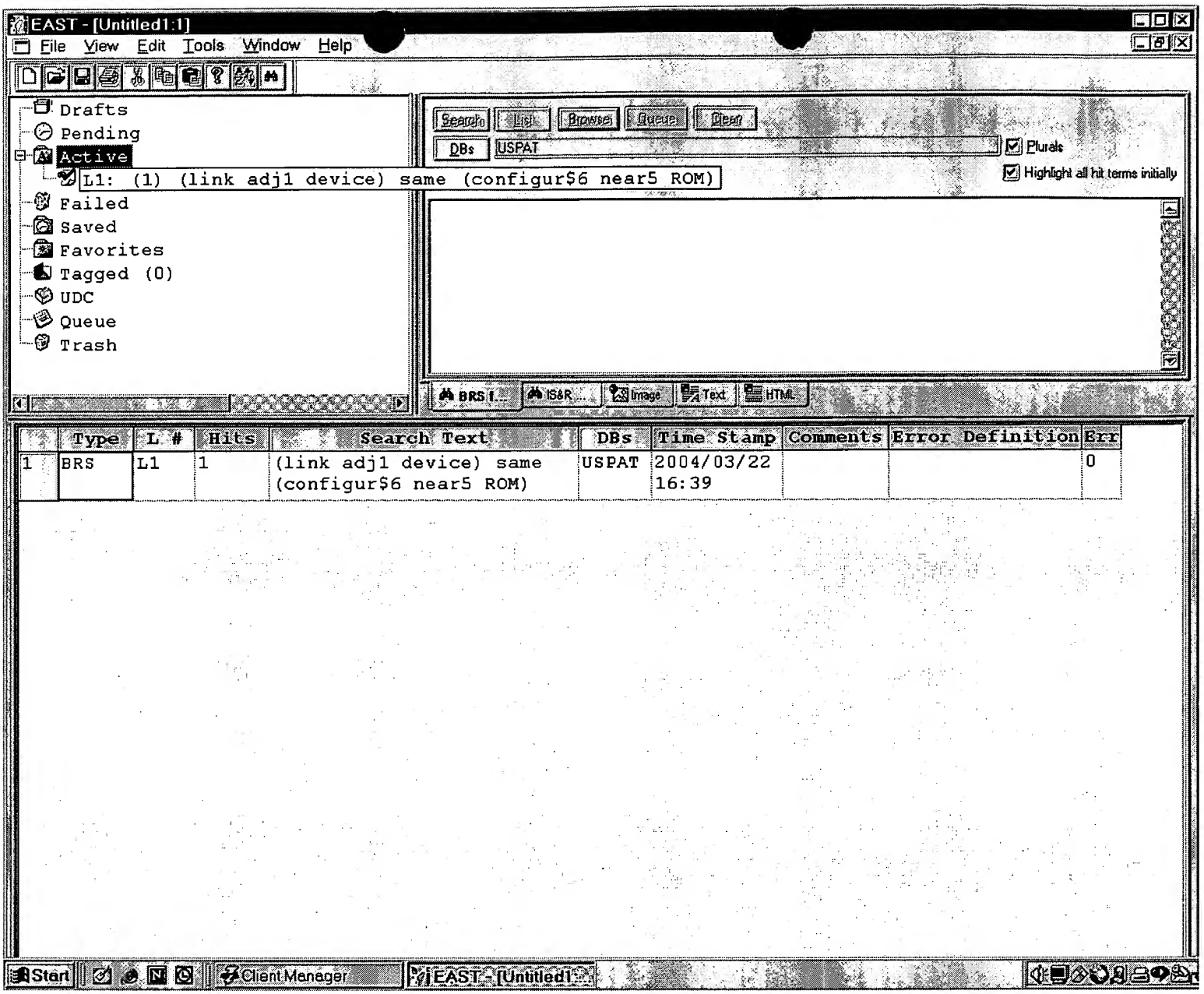
Search History

DATE: Monday, March 22, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=YES; OP=OR		
L4	l1 and L3	15	L4
L3	710/104,105,106,62,63.2,305,8;709/253,301,302,220;370/463;714/1;358/1.15.ccls.	5718	L3
	DB=USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L2	L1	0	L2
	DB=USPT; PLUR=YES; OP=OR		
L1	node same (configur$6 near5 ROM) same (serial adj1 bus)	26	L1

END OF SEARCH HISTORY

h e b b cg b e e ch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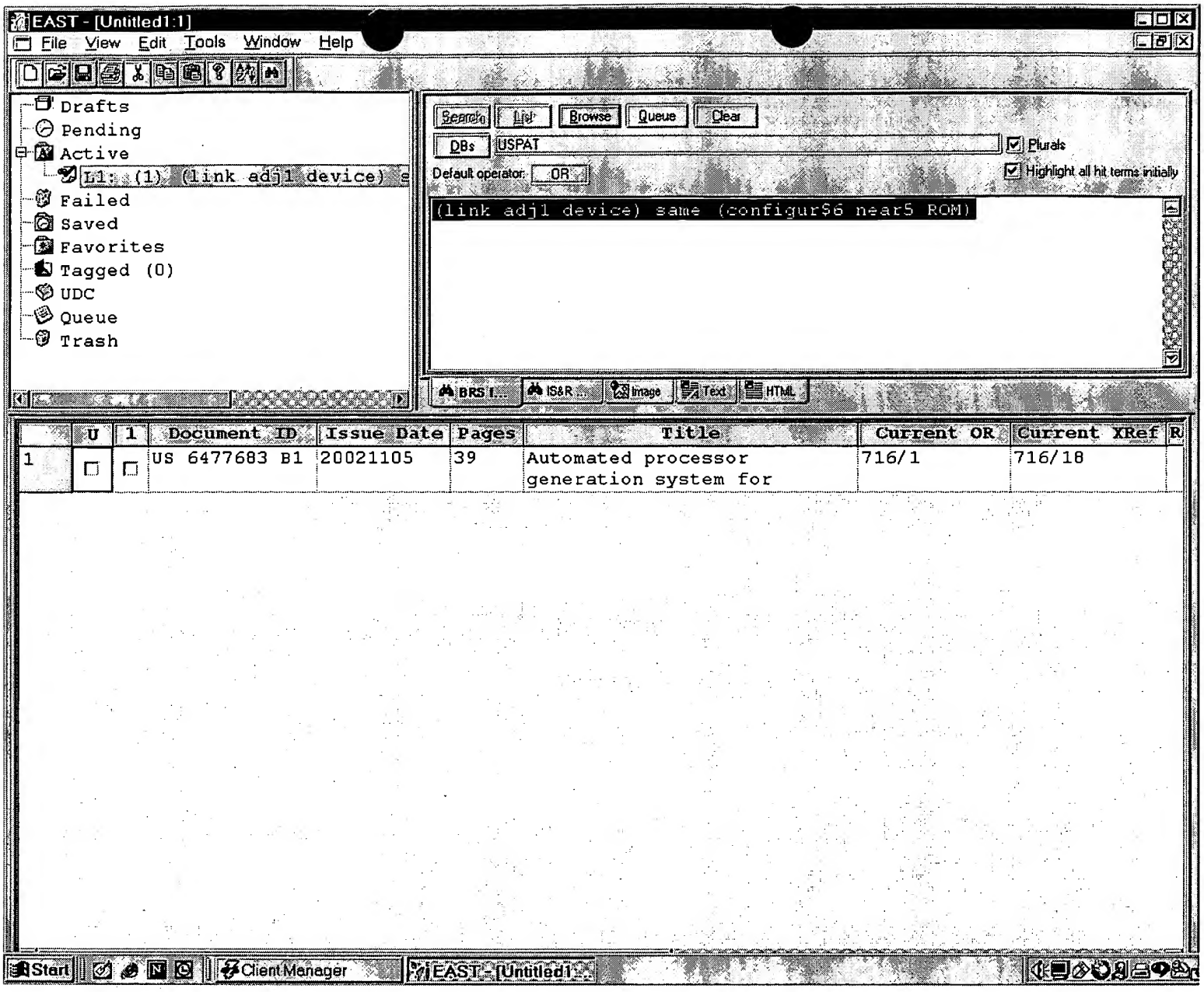
File View Edit Tools Window Help
Drafts
Pending
Active
L1: (1) (link adj1 device) same (configur$6 near5 ROM)
Failed
Saved
Favorites
Tagged (0)
UDC
Queue
Trash
Search
List
Browse
Queue
Clear
DBs
USPAT
Plurals
Highlight all hit terms initially
BRS I...
IS&R...
Image
Text
HTML
Type L # Hits Search Text DBs Time Stamp Comments Error Definition Err
1 BRS L1 1 (link adj1 device) same (configur$6 near5 ROM) USPAT 2004/03/22 16:39 0
Start
Client Manager
EAST - [Untitled1:...


EAST - [Untitled1:1]
File View Edit Tools Window Help
Drafts
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Active
L1: (1) (link adj1 device) s
Failed
Saved
Favorites
Tagged (0)
UDC
Queue
Trash
Search
List
Browse
Queue
Clear
DBs
USPAT
Plurals
Default operator:
OR
Highlight all hit terms initially
(link adj1 device) same (configur$6 near5 ROM)
BRS I...
IS&R ...
Image
Text
HTML
U
1
Document ID
Issue Date
Pages
Title
Current OR
Current XRef
R
1
US 6477683 B1
20021105
39
Automated processor generation system for
716/1
716/18
Start
Client Manager
EAST - [Untitled1:...

Your search matched **1** of **1013964** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enter new one in the text box.

(node or (link device))<and> configur* and rom Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **A parallel ultra-high resolution MPEG-2 video decoder for PC cluster based tiled display systems**
Han Chen; Kai Li; Bin Wei;
Parallel and Distributed Processing Symposium., Proceedings International, IP 2002, Abstracts and CD-ROM , 15-19 April 2002
Pages:15 - 22

[Abstract] [PDF Full-Text (450 KB)] **IEEE CNF**

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Your search matched **0** of **1013964** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enter new one in the text box.

(node or (link device))<and>(configur* rom) Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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Results:
No documents matched your query.

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A parallel ultra-high resolution MPEG-2 video decod PC cluster based tiled display systems

Han Chen Kai Li Bin Wei
Princeton Univ., NJ, USA;

This paper appears in: **Parallel and Distributed Processing Symposium., Proceedings International, IPDPS 2002, Abstracts and CD-ROM**

Meeting Date: 04/15/2002 - 04/19/2002
Publication Date: 15-19 April 2002
Location: Ft. Lauderdale, FL USA
On page(s): 15 - 22
Reference Cited: 14
Number of Pages: CD-ROM
Inspec Accession Number: 7342286

Abstract:
This paper presents a hierarchical parallel MPEG-2 decoder for playing ultra-h resolution videos on PC cluster based tiled display systems. To maximize para while minimizing the communication requirements for a PC cluster, our algorit two-level splitter approach, where a root splitter splits an MPEG-2 video strea picture level and passes them to k second-level splitters, each of which splits into macroblocks and sends them to m × n decoders according to their screer Our experiments with various **configurations** show that this system is highly and has a low and balanced communication requirement among the PC **node** 4 display wall system driven by 21 PCs, the implementation can play back a 3 video at 38.9 frames per second

Index Terms:
computer displays decoding video coding PC cluster based tiled display systems hi parallel MPEG-2 decoder macroblocks parallel ultra-high resolution MPEG-2 video de level splitter approach ultra-high-resolution videos

Documents that cite this document
There are no citing documents available in IEEE Xplore at this time.

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L4: Entry 9 of 15 File: USPT Oct 31, 2000

DOCUMENT-IDENTIFIER: US 6141767 A
TITLE: Method of and apparatus for verifying reliability of contents within the configuration ROM of IEEE 1394-1995 devices

Brief Summary Text (8):
Each node on the IEEE 1394-1995 serial bus provides an identification or configuration read only memory (ROM) in either a minimal or general format. The minimal ROM format includes a single quadlet (4 bytes) of data and provides only a twenty-four (24) bit company identifier. The general ROM format provides other information in addition to the company identifier. The company identifier is used to uniquely identify vendors that manufacture or specify components that are compatible with the IEEE 1394-1995 standard.

Detailed Description Text (5):
While any appropriate device can implement a node, serve as a host system and display the graphical user interface, an exemplary computer system 18 implementing such a node is illustrated in FIG. 6. Preferably, the host system of the present invention is coupled to an IEEE 1394-1995 serial bus network. However, it should be apparent to those skilled in the art that the node of the present invention can be configured to couple to any appropriate bus or network structure. The computer system 18 includes a central processor unit (CPU) 20, a main memory 30, a video memory 22 and an IEEE 1394-1995 interface circuit 28, all coupled together by a conventional bidirectional system bus 34. The interface circuit 28 includes a configuration ROM 29 and a physical interface circuit 42 for sending and receiving communications on the IEEE 1394-1995 serial bus network. The physical interface circuit 42 includes ports which are preferably each configured to be coupled to IEEE 1394-1995 cables connected to other devices. The physical interface circuit is coupled to a television 46 by the IEEE 1394-1995 serial bus cable 45 and to a video camera 44 by the IEEE 1394-1995 serial bus cable 43.

Current US Original Classification (1):
714/1

First Hit Fwd Refs

Generate Collection Print

L4: Entry 9 of 15 File: USPT Oct 31, 2000

US-PAT-NO: 6141767
DOCUMENT-IDENTIFIER: US 6141767 A

TITLE: Method of and apparatus for verifying reliability of contents within the configuration ROM of IEEE 1394-1995 devices

DATE-ISSUED: October 31, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hu; Qi	Santa Clara	CA		
Shima; Hisato	Saratoga	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Sony Corporation	Tokyo			JP	03
Sony Electronics, Inc.	Park Ridge	NJ			02

APPL-NO: 09/ 055132 [PALM]
DATE FILED: April 3, 1998

INT-CL: [07] G06 F 11/00

US-CL-ISSUED: 714/1; 365/201
US-CL-CURRENT: 714/1; 365/201

FIELD-OF-SEARCH: 714/1, 714/2, 714/5, 714/7, 714/20, 714/25, 714/27, 714/31, 714/39, 714/54, 714/4, 714/30, 714/718, 714/736, 365/185.22, 365/201, 364/491

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4238852	December 1980	Iga et al.	371/40
☐	4726028	February 1988	Himeno	371/37
☐	4788684	November 1988	Kawaguchi et al.	371/21
☐	4881232	November 1989	Sako et al.	371/37.4
☐	4910736	March 1990	Tanaka et al.	371/37.7
☐	5001714	March 1991	Stark et al.	371/26

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☐	5020011	May 1991	Stark et al.	364/580
☐	5517508	May 1996	Scott	371/37.1
☐	5577219	November 1996	Timko et al.	395/411
☐	5627955	May 1997	Gnirss et al.	395/141
☐	5644709	July 1997	Austin	395/185.06
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☐	5815509	September 1998	Deng et al.	371/21.2

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IEEE, "1394-1995 Standard for a High Performance Serial Bus," 1995, USA.
ISO/IEC 13213:1994, ANSI/IEEE Std 1212 Cl. 8, 1994, pp. 79-100, USA.

ART-UNIT: 275

PRIMARY-EXAMINER: Iqbal; Nadeem

ATTY-AGENT-FIRM: Haverstock & Owens LLP

ABSTRACT:

A graphical user interface is used to display contents of a configuration memory and includes a hierarchical window illustrating directories and entries within the configuration memory including the relationships between the directories and entries and a data window for displaying data stored within the configuration memory and signalling errors corresponding to the data. The errors are determined by processing the data being displayed to determine a reference value for each entry within the data and to determine if any offset value, pointer value and count value included within any entry references a memory location outside of a boundary of the memory. The reference value specifies a number of times each entry is referenced. Errors are signalled within the data window by displaying entries corresponding to errors in a first color and entries which do not include errors in a second color. The system further includes a bus structure node circuit for coupling the system to other devices over a bus structure. Appropriate headings of directories and entries are displayed with the data in the data window. The bus structure is preferably an IEEE 1394-1995 serial bus.

30 Claims, 14 Drawing figures

US006477683B1

(12) **United States Patent**
Killian et al.

(10) **Patent No.: US 6,477,683 B1**
(45) **Date of Patent: Nov. 5, 2002**

(54) **AUTOMATED PROCESSOR GENERATION SYSTEM FOR DESIGNING A CONFIGURABLE PROCESSOR AND METHOD FOR THE SAME**

(75) Inventors: **Earl A. Killian**, Los Altos Hills, CA (US); **Ricardo E. Gonzalez**, Menlo Park, CA (US); **Ashish B. Dixit**, Mountain View, CA (US); **Monica Lam**, Menlo Park, CA (US); **Walter D. Lichtenstein**, Belmont, MA (US); **Christopher Rowen**, Santa Cruz, CA (US); **John C. Ruttenberg**, Newton, MA (US); **Robert P. Wilson**, Palo Alto, CA (US); **Albert Ren-Rui Wang**, Fremont, CA (US); **Dror Eliezer Maydan**, Palo Alto, CA (US)

(73) Assignee: **Tensilica, Inc.**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/246,047**

(22) Filed: **Feb. 5, 1999**

(51) **Int. Cl.**[7] **G06F 17/50**
(52) **U.S. Cl.** **716/1**; 716/18
(58) **Field of Search** 716/1–21; 712/32, 712/36, 37, 41, 23, 15, 1

(56) **References Cited**

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Hartoog et al, "Generaion of Sotware Tools from Processor Descriptions for Hardware/Software Codesign," ACM, Jun. 1997, pp. 303–306.*
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Fauth et al. "Describing Instruction Set Processors Using nML" (Proc. Euro. Design & Test Conf., Paris, Mar. 1995, IEEE 1995, 5 pp.).
Internet Publication http://www.retarget.com/brfchsch-k.html (19 pp) No date.
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Internet Publication http://www.synopsys.com/products/designware/dwpci_ds.html (16 pp) No date.

(List continued on next page.)

Primary Examiner—Vuthe Siek
(74) *Attorney, Agent, or Firm*—Pillsbury Winthrop LLP

(57) **ABSTRACT**

An automated processor design tool uses a description of customized processor instruction set extensions in a standardized language to develop a configurable definition of a target instruction set, a Hardware Description Language description of circuitry necessary to implement the instruction set, and development tools such as a compiler, assembler, debugger and simulator which can be used to develop applications for the processor and to verify it. Implementation of the processor circuitry can be optimized for various criteria such as area, power consumption, speed and the like. Once a processor configuration is developed, it can be tested and inputs to the system modified to iteratively optimize the processor implementation. By providing a constrained domain of extensions and optimizations, the process can be automated to a high degree, thereby facilitating fast and reliable development.

104 Claims, 12 Drawing Sheets

US-PAT-NO: 6477683

DOCUMENT-IDENTIFIER: US 6477683 B1

TITLE: Automated processor generation system for designing a configurable processor and method for the same

---------- KWIC ----------

Detailed Description Text - DETX (121):

The emulation board 200 has several resources available on it to allow for easy software development, debugging and verification. These include the CPLD device 202 itself, EPROM 204, SRAM 206, synchronous SRAM 208, flash memory 210 and two RS232 serial channels 212. The serial channels 212 provide a communication link to UNIX or PC hosts for downloading and debugging user programs. The configuration of a processor 60, in terms of the CPLD netlist, is downloaded into the CPLD 202 through a dedicated serial link to device's configuration port 214 or through dedicated configuration ROMs 216.

L3: Entry 1 of 32 File: USPT Mar 9, 2004

DOCUMENT-IDENTIFIER: US 6704819 B1
TITLE: Method and apparatus for device sharing and arbitration

Detailed Description Text (6):
An additional serial port in the form of an IEEE 1394 interface 142 may also be provided. The IEEE 1394 interface 142 couples an IEEE 1394-compliant serial bus 145 to the system bus 130 or similar communication bus. The IEEE 1394-compliant serial bus 145, as known in the art, allows devices 152 and other computers 151 to communicate with the computer 100 and each other using high-speed serial channels. The IEEE 1394 serial bus standard is based largely upon the internationally adopted ISO/IEC 13213 (ANSI/IEEE 1212) CSR Architecture Specification and the IEEE 1394-1995 Serial Bus Specification, the teachings of which are herein incorporated by these references. A typical serial bus having an IEEE 1394 standard architecture is comprised of a multiplicity of nodes that are interconnected via point-to-point links, such as cables, that each connect a single node of the serial bus to another node of the serial bus. The nodes themselves are addressable entities that can be independently reset and identified. Each node provides a so-called configuration ROM (read-only memory) or configuration memory and a standardized set of control registers that can be accessed by software residing within the computer system. The configuration memory of a given node provides, in part, a description of the functional capabilities of that node. The configuration memory for each node residing on the serial bus is exposed to all other nodes. During a configuration process, other nodes access each node's configuration memory (a process often referred to as "enumerating") in order to determine the proper system configuration. Thus, one function of the configuration memory of a given node is to instruct other nodes as to the given node's functional capabilities, thereby allowing the other nodes to determine which device drivers to load. As known in the art, each device has an associated driver that, among other functions, configures the device and allows the device to be operable within the overall system. Drivers are typically software instructions that can be loaded into a computer's memory that, when executed, will communicate with the corresponding device to properly configure the device for operation. The driver may initialize the device so that the device can function and the driver may also allow the device to communicate with higher protocol levels within the computer.

First Hit Fwd Refs

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L3: Entry 1 of 32 File: USPT Mar 9, 2004

US-PAT-NO: 6704819
DOCUMENT-IDENTIFIER: US 6704819 B1

TITLE: Method and apparatus for device sharing and arbitration

DATE-ISSUED: March 9, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chrysanthakopoulos; Georgios	Kirkland	WA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Microsoft Corporation	Redmond	WA			02

APPL-NO: 09/ 553453 [PALM]
DATE FILED: April 19, 2000

INT-CL: [07] G06 F 1/00

US-CL-ISSUED: 710/240; 710/200, 710/309
US-CL-CURRENT: 710/240; 710/200, 710/309

FIELD-OF-SEARCH: 710/306, 710/309, 710/311, 710/313, 710/316, 710/240, 710/243, 710/244, 710/315, 710/15, 710/16, 710/110, 710/113, 710/200, 709/208, 709/209, 709/211, 709/219, 709/227, 709/250

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5317693	May 1994	Cuenod et al.	710/305
☐	5805905	September 1998	Biswas et al.	710/260
☐	5938752	August 1999	Leung et al.	710/126
☐	6018785	January 2000	Wenniger	710/200
☐	6038625	March 2000	Ogino et al.	710/104
☐	6105094	August 2000	Linderman	710/107
☐	6115770	September 2000	Gehman	710/128

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☐	6141702	October 2000	Ludtke et al.	710/5
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☐	6366964	April 2002	Shima et al.	710/8
☐	6378000	April 2002	Akatsu et al.	709/245
☐	6385679	May 2002	Duckwall et al.	710/119
☐	6389502	May 2002	Toguchi	710/314
☐	6389560	May 2002	Chew	714/43
☐	6434117	August 2002	Momona	370/236
☐	6519657	February 2003	Stone et al.	710/306
☐	6519671	February 2003	Kondou et al.	710/311
☐	6529984	March 2003	Tenner et al.	710/240

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FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0827062	April 1998	EP	
0930747	July 1999	EP	
1217787	June 2002	EP	

ART-UNIT: 2181

PRIMARY-EXAMINER: Myers; Paul R.

ASSISTANT-EXAMINER: Phan; Raymond N

ATTY-AGENT-FIRM: Banner & Witcoff, Ltd.

ABSTRACT:

In a system in which control-capable nodes are coupled to each other and one or more devices via a communications bus, the control-capable nodes determine the identity of an owner node of a given device and register with the owner node for notification of changes to the device's ownership. The control-capable nodes may request ownership from the owner node, which request may be granted or denied, or the control-capable nodes may detect that ownership by the owner node has terminated. It such a request is granted, or if such termination is detected, the control-capable nodes attempt to establish ownership of the device according to previously assigned priorities. Data structures supporting these operations provide communications between device drivers and bus drivers in a control-capable node, and provide communications between bus drivers in different control-capable nodes. In this manner, the present invention provides a technique for device arbitration that does not require modifications to, nor participation by, the controlled devices.

33 Claims, 4 Drawing figures

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L3: Entry 14 of 32 File: USPT Nov 5, 2002

DOCUMENT-IDENTIFIER: US 6477589 B1
TITLE: Information processing apparatus and method

Detailed Description Text (119):
On the other hand, the configuration ROM itself and the function for reading the configuration ROM are necessarily installed in a device adapted to or based on the IEEE 1394 standard. Accordingly, by storing information on device position, device function and the like in the configuration ROM of the respective nodes, and providing a function to read these information from application software, a so-called device map display function can be realized in the application software of the respective node independent of a specific protocol for data base access, data transfer or the like. in the configuration ROM, physical position information or function information can be stored as node unique information, and can be used for realizing the device map display function.

Detailed Description Text (120):
In this manner, the application software reads the information from the configuration ROM of each node, upon bus reset or in response to a request from a user, and obtains the topology of the 1394 network by physical positional relation. Further, the application software obtains the function information of each node with the physical position information of the node by reading the various node information on the functions and the like, described in the configuration ROM.

Detailed Description Text (121):
When the application software obtains the information in the configuration ROM of each node, an application interface (API) is employed to obtain the information in an arbitrary configuration ROM of a designated node. By using this means, the application software on the device on the 1394 network generates various device maps and lists such as a physical topology map and a map of functions of the respective nodes, in accordance with purposes. Further, it is possible for the user to select a device having a necessary function, by using the application software.

Detailed Description Text (190):
Each of devices according to/corresponding to the present embodiment can store and hold location information of the node, with its node unique information, in a predetermined format, into a position information entry (Position info entry) of the node dependent information directory (Node Dependent Info Directory) 1003 of the configuration ROM.

Detailed Description Text (191):
As shown in FIG. 43, each node can store and hold function change information, with its node unique information, in a predetermined format, in a function information generation entry (Function info generation entry) of the node dependent information directory (Node Dependent Info directory) 1003 of the configuration ROM.

Detailed Description Text (197):
As shown in FIG. 43, each node can store the status of use and connection status of itself, in a predetermined format, into the use information entry (Use info entry) and the connection information entry (Connection info entry) of the node dependent information directory (Node Dependent Info Directory) 1003 of its configuration

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ROM. The status of use, connection status and record of use of the node can be obtained by reading these information.

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First Hit Fwd Refs

Generate Collection Print

L3: Entry 14 of 32 File: USPT Nov 5, 2002

US-PAT-NO: 6477589
DOCUMENT-IDENTIFIER: US 6477589 B1

TITLE: Information processing apparatus and method

DATE-ISSUED: November 5, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Suzuki; Naohisa	Yokohama			JP
Nakamura; Atsushi	Kawasaki			JP
Kobayashi; Makoto	Yokohama			JP
Katano; Kiyoshi	Chiba			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Canon Kabushiki Kaisha	Tokyo			JP	03

APPL-NO: 09/ 270210 [PALM]
DATE FILED: March 15, 1999

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	10-063665	March 13, 1998
JP	11-066329	March 12, 1999

INT-CL: [07] G06 F 3/00

US-CL-ISSUED: 710/18; 710/9, 710/10, 710/19
US-CL-CURRENT: 710/18; 710/10, 710/19, 710/9

FIELD-OF-SEARCH: 710/18, 710/9, 710/10, 710/19, 710/8

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5353399	October 1994	Kuwamoto et al.	395/159
☐	5832298	November 1998	Sanchez et al.	710/8

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☐	6044411	March 2000	Berglund et al.	710/9

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0 745 929	December 1996	EP	

OTHER PUBLICATIONS

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ART-UNIT: 2181

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ABSTRACT:

In a 1394 network where a number of devices are connected, it is not easy to specify corresponding between a displayed device and a real device. Accordingly, "selection-candidate update processing, to find a new device and "processing for displaying candidates meeting set conditions" to display candidates which meet set conditions are provided, so as to display a device list window displaying selection candidates in a case where a set condition is, e.g., "printer".

26 Claims, 64 Drawing figures